AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of the Claims

1-19. (Canceled).

20. (Currently Amended) A MOS transistor, comprising:

a T-shaped gate electrode ~~disposed~~ on a semiconductor substrate, the T-shaped gate electrode having a wide portion and a narrow portion, the narrow portion ~~disposed~~ between the wide portion and the semiconductor substrate, so as to have an undercut region adjacent to the narrow portion;

an L-shaped lower spacer covering a top surface of the semiconductor substrate at both sides of the T-shaped gate electrode and covering sides of the wide portion of the T-shaped gate electrode, the L-shaped lower spacer having a first element ~~disposed~~ substantially perpendicular to the semiconductor substrate, ~~and having~~ a second element, having substantially the same thickness as the first element, ~~disposed~~ substantially parallel to the semiconductor substrate, the second element extending from the first element laterally away from the T-shaped gate electrode, and a third element substantially parallel to the semiconductor substrate extending from a bottom of the first element into the undercut region, wherein the first element and the second element intersect to define a substantially 90 degree angle in an outer surface of the L-shaped lower spacer;

a low-concentration impurity region ~~formed~~ in the semiconductor substrate ~~at both sides of the T-shaped gate electrode~~ substantially under the first and third elements;

a high-concentration impurity region ~~formed~~ in the semiconductor substrate next to the L-shaped lower spacer; and

a mid-concentration impurity region ~~disposed~~ between the high- and low-concentration impurity regions, substantially under the second element.

21. (Currently Amended) The MOS transistor as claimed in claim 20, wherein the T-shaped gate electrode comprises:

lower and upper conductive layer patterns that are sequentially stacked, wherein the upper conductive layer pattern is wider than the lower conductive layer pattern to define the undercut region.

22. (Canceled).

23. (Original) The MOS transistor as claimed in claim 21, wherein the lower and upper conductive layer patterns are made of materials having an etch selectivity with respect to each other.

24. (Original) The MOS transistor as claimed in claim 21, wherein the lower conductive layer pattern is made of silicon germanium or nitride titanium.

25. (Original) The MOS transistor as claimed in claim 21, wherein the upper conductive layer pattern is made of polysilicon or tungsten.

26. (Currently Amended) A MOS transistor, comprising:

a T-shaped gate electrode ~~disposed~~ on a semiconductor substrate, the T-shaped gate electrode having a wide portion and a narrow portion, the narrow portion ~~disposed~~ between the wide portion and the semiconductor substrate, so as to have an undercut region adjacent

to the narrow portion;

an L-shaped lower spacer covering a top surface of the semiconductor substrate at both sides of the T-shaped gate electrode and covering sides of the wide portion of the T-shaped gate electrode, the L-shaped lower spacer having a first element ~~disposed~~ substantially perpendicular to the semiconductor substrate, ~~and having~~ a second element, having substantially the same thickness as the first element, ~~disposed~~ substantially parallel to the semiconductor substrate, the second element extending from the first element laterally away from the T-shaped gate electrode, and a third element substantially parallel to the semiconductor substrate extending from a bottom of the first element into the undercut region, wherein the first element and the second element intersect to define a substantially 90 degree angle in an outer surface of the L-shaped lower spacer;

a low-concentration impurity region ~~formed~~ in the semiconductor substrate ~~at both sides of the T-shaped gate electrode~~ substantially under the first and third elements;

a high-concentration impurity region ~~formed~~ in the semiconductor substrate next to the L-shaped lower spacer;

a mid-concentration impurity region ~~disposed~~ between the high- and low-concentration impurity regions, substantially under the second element, and

a surface insulating layer intervened between the narrow portion of the gate electrode and the L-shaped lower spacer.

27-30. (Canceled).

31. (Previously Presented) The MOS transistor as claimed in claim 26, wherein the surface insulating layer partially, but not completely, fills the undercut region and the L-shaped lower spacer completely fills the remainder of the undercut region.

32. (Previously Presented) The MOS transistor as claimed in claim 20, wherein a width of the first element, which is measured beside the T-shaped gate electrode, is substantially equal to a thickness of the second element, which is measured on the mid-concentration impurity region.

33. (Previously Presented) The MOS transistor as claimed in claim 26, wherein a width of the first element, which is measured beside the T-shaped gate electrode, is substantially equal to a thickness of the second element, which is measured on the mid-concentration impurity region.

34. (New) The MOS transistor as claimed in claim 26, wherein the surface insulating layer is an insulating layer having an etch selectivity with the L-spaced spacer.

35. (New) The MOS transistor as claimed in claim 34, wherein the surface insulating layer is a thermal oxide and the L-shaped spacer is at least one of nitride, oxynitride, and polysilicon.

36. (New) The MOS transistor as claimed in claim 20, further comprising a surface insulating layer between the gate electrode and the L-shaped spacer.

37. (New) The MOS transistor as claimed in claim 36, wherein the surface insulating layer partially, but not completely, fills the undercut region and the third element of the L-shaped spacer completely fills the remainder of the undercut region.

38. (New) The MOS transistor as claimed in claim 36, wherein the surface insulating layer is an insulating layer having an etch selectivity with the L-shaped spacer.

39. (New) The MOS transistor as claimed in claim 38, wherein the surface insulating layer is a thermal oxide and the L-shaped spacer is at least one of nitride, oxynitride, and polysilicon.

40. (New) A MOS transistor comprising:

a T-shaped gate electrode on a semiconductor substrate, the T-shaped gate electrode having a narrow portion and a wide portion, which are stacked sequentially, to define an undercut region between the wide portion and the semiconductor substrate;

an L-shaped spacer locally at both sides of the T-shaped gate electrode, the L-shaped spaced having a first element substantially perpendicular to the semiconductor substrate, a second element extending away from a bottom of the first element, substantially parallel to the semiconductor substrate, and having substantially the same thickness as the first element, and a third element extending from the bottom of the first element, substantially parallel to the semiconductor substrate to partially fill the undercut region; and

a surface insulating layer between the gate electrode and the L-shaped spacer to fill the remainder of the undercut region,

wherein the surface insulating layer is an insulating layer having an etch selectivity with the L-spaced spacer.

41. (New) The MOS transistor as claimed in claim 40, wherein the surface insulating layer is a thermal oxide and the L-shaped spacer is at least one of nitride, oxynitride, and polysilicon.